



1 / 6

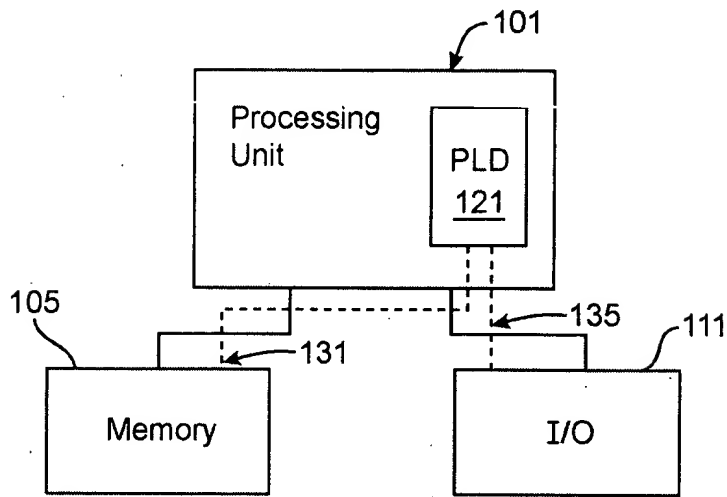


FIG. 1

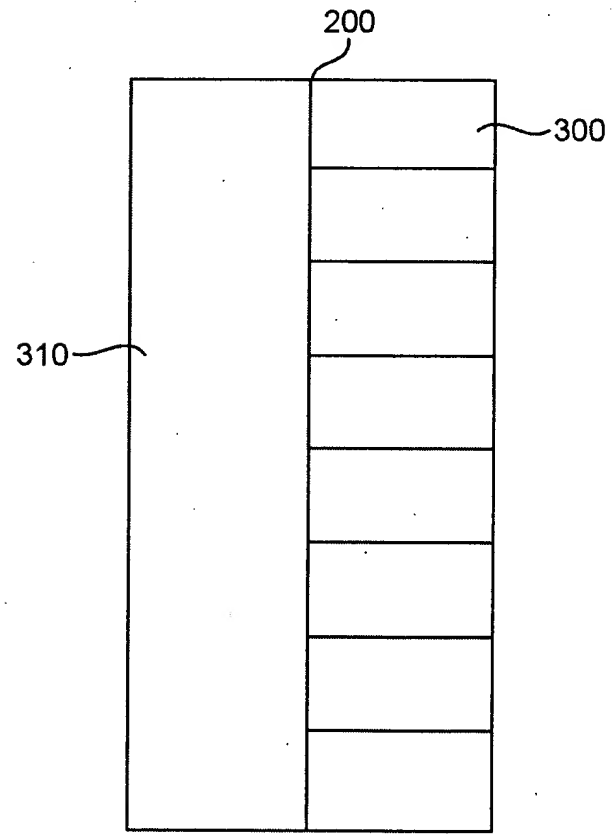


FIG. 3

(650) 324-8371 015114-053400US  
Atty: Steven J. Cahill Reg. No. 44,578  
I/O CIRCUITRY SHARED BETWEEN PROCESSOR AND PROGRAMMABLE  
LOGIC PORTIONS OF AN INTEGRATED CIRCUIT  
Roger May et al. 09/880,458  
Sheet 2 of 6

The diagram illustrates a logic array architecture with the following components and connections:

- I/O Element (IOE):** Represented by boxes at the top and bottom edges.
- Embedded Array Block (EAB):** Shaded vertical blocks on the left and right sides that interface IOEs with the internal array.
- Column Interconnect:** A central vertical bus that routes signals between columns of Logic Array Blocks.
- Row Interconnect:** A central horizontal bus that routes signals between rows of Logic Array Blocks.
- Logic Array Block (LAB):** The primary processing units arranged in a grid.
- Logic Array:** A dashed rectangular region encompassing multiple LABs.
- Logic Element (LE):** Individual components within a LAB.
- Local Interconnect:** Internal routing within a LAB or Logic Array.
- Embedded Array:** The overall grid structure of LABs.



4 / 6

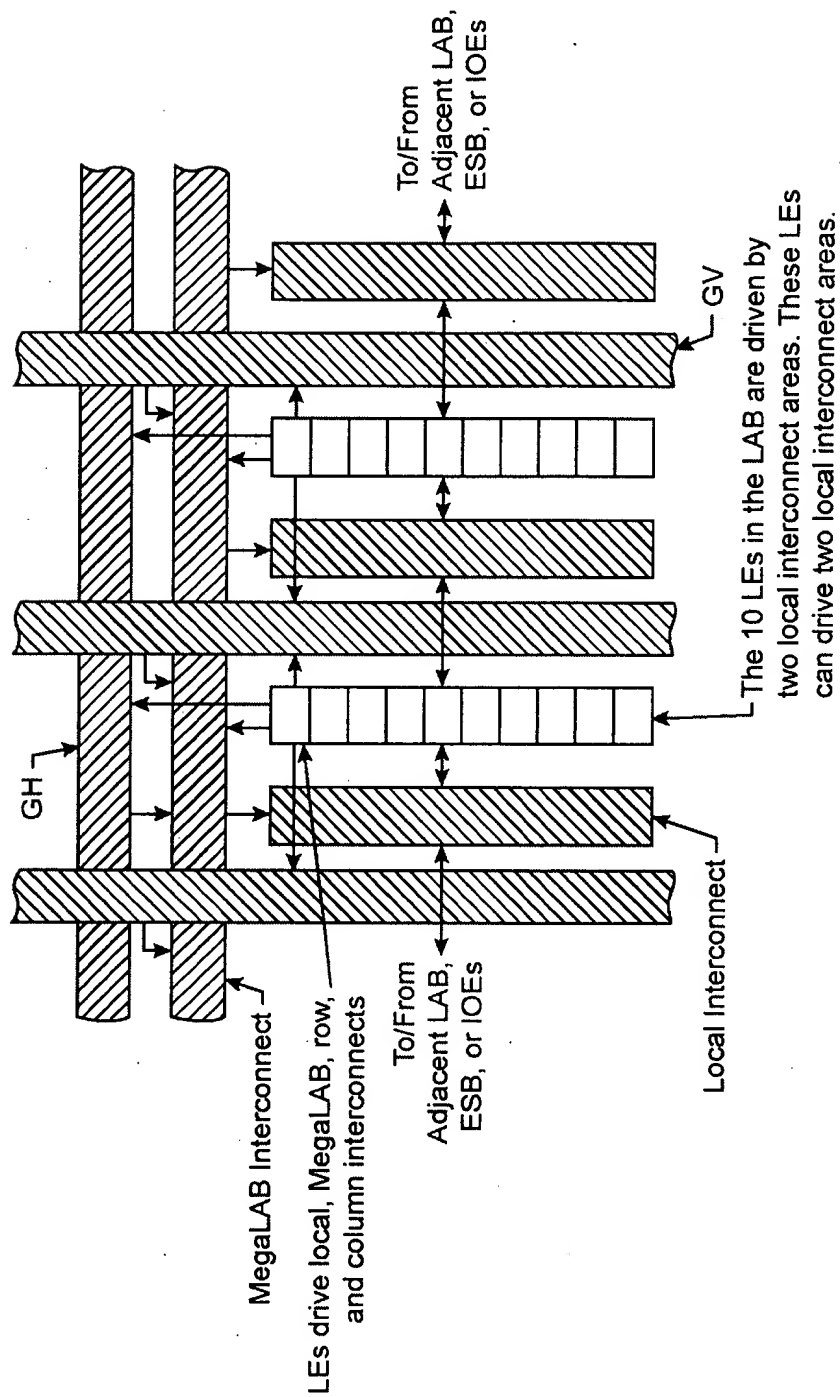


FIG. 5



5 / 6

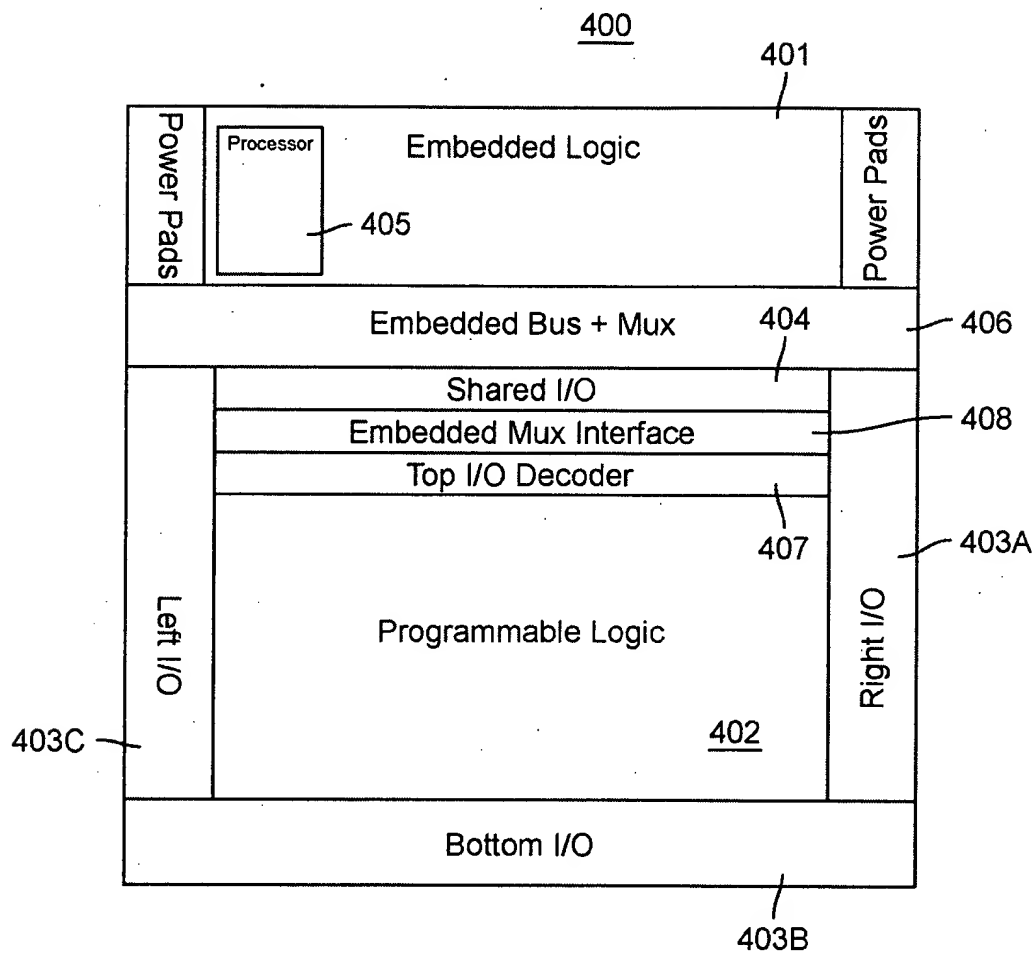


FIG. 6



6 / 6

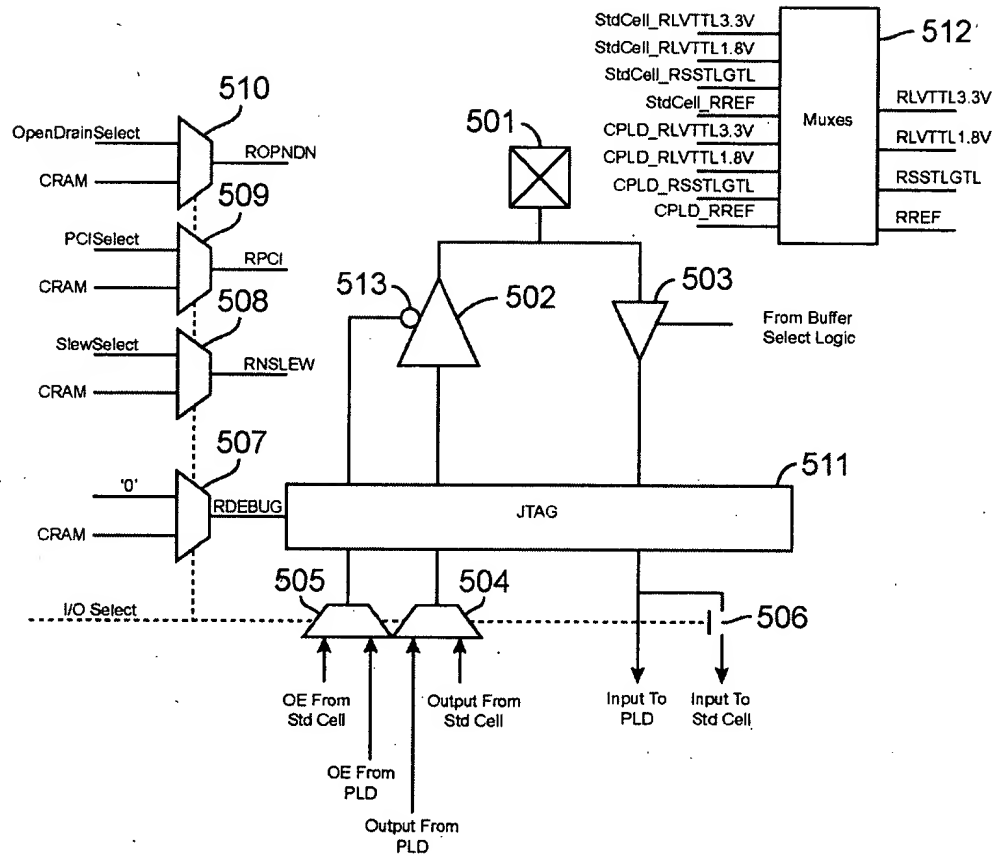


FIG. 7